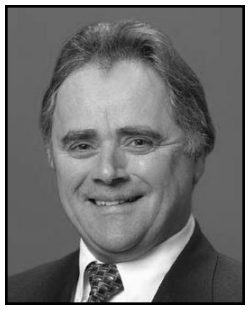
SE5 Highlights of IEDM 2006



Organizer: Albert Theuwissen, DALSA, Eindhoven, The Netherlands
Chair: Ernesto Perea, ST Microelectronics, Crolles, France

IEDM is the most important international forum for advances in solid-state devices and breakthrough in semiconductor technology, and is fully supported by the IEEE Electron Devices Society. Amongst the IEDM papers presented at IEDM2006, following a very rigorous selection process, four papers were invited to be presented at ISSCC this year.

It is the very first time that IEDM papers will be presented at the ISSCC. The main reason for doing this is to bring the circuitry engineers close to the forefront of device and technology developments. Both worlds of devices and circuits have so much in common that one cannot live without the other. In this special evening session we try to bring both worlds together.

Three Dimensionally Stacked NAND Flash Memory Technology Using Stacking Single Crystal Si Layers on ILD and TANOS Structure for Beyond 30nm Node

Soon-Moon Jung, et al., Samsung, Yogin-City, Kyungki-do, Korea,

Three dimensionally stacked NAND flash memory cell arrays are formed on the ILD as well as on the bulk to double the memory density without increasing the chip size, by implementing S^3 technology. The feasibility of the technology was proven by the successful operations of 32 bit NAND flash memory cell strings with 63nm dimensions, TANOS structures, and the novel SBT (Source-Body Tied) operational scheme.

Doubling or Quadrupling MuGFET fin Integration Scheme with Higher Pattern Fidelity, Lower CD Variation and Higher Layout Efficiency

Rita Rooyackers, et al., IMEC, Leuven, Belgium,

Multiple Gate Field Effect Transistors (MuGFET) with fin quadrupling by adding two operations to the fin doubling module are demonstrated. Due to the 50nm fin pitch, selective epitaxial growth silicon (SEG-Si) will connect the fins outside the spacer region reducing the high parasitic source/drain-resistance (R_{SD}) and resulting in higher drive current per surface unit.

A Cost-Effective Low Power Platform for the 45-nm Technology Node

Olivier Callen, et al., STMicroelectronics, Crolles, France,

The paper presents a cost-effective 45nm technology platform, primarily designed to serve the wireless multimedia and consumer electronics needs. This platform features low power transistors operating at a nominal voltage of 1.1V, an ultra low k dielectric (k = 2.5) with up to 9 Cu metal layers and 0.25/0.3/0.37μm^2 SRAM cells. This platform also features an optional third gate oxide for either higher speed or active power mitigation. This technology has been developed on the (100)-oriented substrate with a key focus on process simplicity. Transistor improvement relies on mask-free strain engineering techniques along with co-implanted halos and laser anneal. The impact of laser anneal on transistor reliability and mixed-signal capabilities are also examined. Drive current as high as 660/320 mA/mm and 1.1 V are reported.

Ultra-Thin Phase-Change Bridge Memory Device Using GeSb

Y.C. Chen, et al., IBM Almaden Research Center, San Jose, CA

An ultra-thin phase-change bridge (PCB) memory cell, implemented with doped GeSb, is shown with < 100μA RESET current. The device concept provides for simplified scaling to small cross-sectional area (60nm^2) through ultra-thin (3nm) films; the doped GeSb phase-change material offers the potential for both fast crystallization and good data retention.